REMARKS

Claims 1-14 are pending in the present application. Claims 1-14 stand rejected. Applicants gratefully appreciate the Examiner's indication that claims 3 and 11-12 would be allowable if amended as suggested on page 4 of the Office Action.

Claims 1, 5-6, 8-9, and 13-14 have been amended. Reconsideration of the claim rejections are respectfully requested in view of the following remarks.

Claim Rejections - § 112

Claims 1, 5-6, and 13-14 stand rejected under 35 U.S.C. § 112, second paragraph, for the reasons set forth on page 2 of the Office Action. Claims 1, 5-6, and 13-14 have been amended to address the issues raised by the Examiner. Withdrawal of the rejection under 35 U.S.C. § 112, second paragraph, is respectfully requested.

Claim Rejections - § 102

(1) Claims 1, 4-5, 7-9, and 13-14 stand rejected under 35 U.S.C 102(e) as being anticipated by Sanie (U.S. Pub. 2004/0210856). It is respectfully submitted that Sanie is legally deficient to establish a *prima facie* case of anticipation against claims 1, 4-5, 7-9, and 13-14. At the very least, Sanie does not anticipate claims 1, 13, and 14.

By way of example, with respect to claims 1, 13 and 14, it is submitted that Sanie does not disclose or suggest "*creating a structural metric prior to physical design, the structural metric being proportional to a routability of the circuit design model after the physical design*", as recited *inter alia* in claims 1, 13 and 14.

The Examiner contends (in fig. 3, par. 0043) that Sanie teaches "*creating a structural metric prior to physical design, the structural metric being proportional to a routability of the circuit design model after the physical design.*" However, it is respectfully submitted that Examiner's characterization of the teachings of Sanie in this regard is misplaced. To begin, Sanie does not even disclose the claimed "*structural metric*" in paragraph 0043. The paragraph focuses on a physical processing step 303 which may consider mask cost based on a mask cost metric of figure 3. Although Sanie arguably discloses a mask cost metric (in figure 3), this metric is entirely different from a structural metric which is proportional to a routability of a circuit design. Indeed Sanie explicitly teaches that a mask cost metric (in par. 0008) relates to the cost of "*fabricating a mask set for exposing a wafer that will provide the desired integrated circuit.*" This is further evident by Sanie's teaching of "*a method for providing a mask design that can be optimized for cost*" (in par. 0011) and a further teaching that the method includes a related "*mask cost metric*" (in par. 0012).

Accordingly, claims 1, 13, and 14 are not anticipated by Sanie. Moreover, claims 4-5, and 7-9 are patentable over Sanie at least by virtue of their dependence from claim 1.

(2) Claims 1-2, 4-7, 9-10, and 13-14 stand rejected under 35 U.S.C 102(b) as being anticipated by Higashida (U.S. Pat. 6006023). It is respectfully submitted that Higashida is legally deficient to establish a *prima facie* case of anticipation against claims 1-2, 4-7, 9-10, and 13-14. At the very least, Higashida does not anticipate claims 1, 13 and 14.

By way of example, it is submitted that Higashida does not disclose or suggest "*using the structural metric during logic synthesis to create an optimized circuit design model*", as recited *inter alia* in claims 1, 13, and 14.

The Examiner contends that Higashida teaches (in figs. 1, 11-12, and 17-19) "*using the structural metric during logic synthesis to create an optimized circuit design model.*" It is respectfully reminded that the Examiner has the burden to establish anticipation by showing how Higashida discloses each and every limitation in the claims. The Examiner has simply cited several figures of Higashida without any analysis of the claims or any analysis of the cited figures of Higashida with respect to the claims. It is unclear which elements of which figures of Higashida are specifically relevant to the Examiner's anticipation rejection.

It is not the Applicants burden to show why Higashida does not anticipate the claims. In any event, it is respectfully submitted that Examiner's characterization of the teachings of Higashida is misplaced. Higashida discloses (in col. 5, lines 7-10) performing an "*optimization of [a] logic circuit ... through detection of a symmetry in logic structure after logic synthesis*". Moreover, a first step 101 of figures 1 and 11 is entitled "*input of logic circuit after logic synthesis.*" So even assuming, *arguendo*, that Higashida's "*detection of a symmetry*" is a "*structural metric*", as contemplated by the claimed invention, such a metric is used after logic synthesis and not during logic synthesis as recited *inter alia* in claims 1, 13, and 14. Accordingly, claims 1, 13, and 14 are not anticipated by Higashida. Moreover, claims 2, 4-7, and 9-10 are patentable over Higashida at least by virtue of their dependence from claim 1.

In view of the foregoing remarks, it is respectfully submitted that all the claims now pending in the application are in condition for allowance. Early and favorable reconsideration is respectfully requested.

Respectfully submitted,

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